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10/726,312	12/01/2003	Greg A. Blodgett	501266.01	3071

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/726,312	BLODGETT ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-29,31 and 37-47* is/are allowed.

6)☒ Claim(s) *30,32,33,35, 37,48,50 and 51* is/are rejected.

7)☒ Claim(s) *34,36,49 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/04,11/04,12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1, 6, 13, 21, 23, 38 and 40 are objected to because of the following informalities:

In claim 1, "the driver circuit" on line 8 appears to be --the output driver circuit--;

In claim 6, "output driver circuit" on line 2 appears to be --the output driver circuit--;

In claims 13 and 14, "the counters" on line 2 appears to be --the pull-up and pull-down counters-- respectively;

In claim 21, "output driver circuit" on line 1 appears to be --the output driver circuit--;

In claim 23, "predriver circuits" on line 1 appears to be --first and second predriver circuits--;

In claim 38, "the drive strength bits" on line 8 appears to be --the drive mode bits--;

In claim 40, "the count" on line 3 appears to be --the drive strength count--;

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 30 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 30 recites the limitation "the predriver circuits" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 32 recites the limitation "the drive strength mode bits" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 33, 35, 37, 48 and 50-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Waldrop (US PAT No. 6,885,226).

Regarding claim 33, Figs. 2 and 3 of Waldrop teaches a method of adjusting a drive strength of an output driver (full level or reduced level; col. 1, line 65 - col. 2, line 4) , the method comprising setting a drive strength count (full level or reduced level by FULLDRIVE_PUP, PUP, PDN, FULLDRIVE_PDN counts), storing a drive strength adjustment word (FULL DRIVE, DQHO*,DQLO, DATA bits are from memory array; col. 5, lines 10-14); adjusting the drive strength count as a function of the drive strength adjustment word (FULLDRIVE_PUP, PUP, PDN, FULLDRIVE_PDN counts are adjusted by FULL DRIVE, DQHO*,DQLO, DATA bits); and adjusting the drive strength of the output driver as a function of the drive strength count (strength of the output driver 204 is adjusted by FULLDRIVE_PUP, PUP, PDN, FULLDRIVE_PDN counts).

Regarding claim 35, Figs. 2 and 3 of Waldrop teaches the method of claim 33 where the drive strength adjustment word comprises a four bit word (FULL DRIVE, DQHO*,DQLO, DATA bits).

Regarding clam 37, Figs. 2 and 3 of Waldrop teaches the method of claim 33 where adjusting the drive strength of the output drive as a function of the drive strength adjustment word comprising adjusting an impedance between an output node and a supply voltage source (pull up transistors in Fig. 2 adjust pull-up impedance) and between the output node and a reference voltage source responsive to the drive strength adjustment word source (pull down transistors in Fig. 2 adjust pull-down impedance).

Regarding claim 48, Figs. 2 and 3 of Waldrop teaches a driver adjustment circuit, comprising a predriver circuit (202 in Fig 2) configured to receive a strength code and a data signal (FULL DRIVE, DQHO*,DQLO, DATA) and in response thereto generate a plurality of output driver control signals (FULLDRIVE_PUP, PUP, PDN, FULLDRIVE_PDN); and an output driver circuit (204) coupled to the predriver circuit to receive the plurality of output driver control signals, the output driver circuit operable to develop an output signal on an output node responsive to the data signal having a drive strength as a function of the plurality of output driver control signals (full level or reduced level; col. 1, line 65 - col. 2, line 4).

Regarding claim 50, Figs. 2 and 3 of Waldrop teaches the driver adjustment circuit of claim 48 where the plurality of output driver control signals comprises a plurality of output driver control pull-up signals (FULLDRIVE_PUP, PUP) and a plurality of output driver control pull-down signals (PDN, FULLDRIVE_PDN) generated by the predriver circuit in response to the strength code and data signal.

Regarding claim 51, Figs. 2 and 3 of Waldrop teaches the driver adjustment circuit of claim 50 where the output driver circuit comprises: a pull-up driver circuit (pull up transistors in 204 of Fig. 2) coupled to the predriver circuit to receive the plurality of output driver pull-up signals and operable to determine a pull-up drive strength of an output signal as a function of the plurality of output driver pull-up signals when the output signal is to be driven high (DQPAD is high when the pull up transistors are pulled up high); and a pull-down driver circuit (pull down transistors in 204 of Fig. 2) coupled to the predriver circuit to receive the plurality of output driver pull-down signals and operable to determine a pull-down drive strength of the output signal as a function of the plurality of output driver pull-down signals when the output signal is to be driven low (DQPAD is low when the pull down transistors are pulled down low).

Allowable Subject Matter

Claims 1-29, 31, 38-47 are allowable over the prior art of record.

Claims 34, 36, 49 and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Waldrop teaches programmable dual-drive strength output buffer, one of ordinary skill in the art would not have been motivated to modify the teaching of Waldrop to further includes, among other things, the specific of a counter circuit coupled to the storage circuit to receive the drive strength adjustment word and operable to develop a drive strength count responsive to the drive strength adjustment word as set forth in the claims 1, 15, and 26, the specifics of a first predriver adapted to receive a data signal and coupled the pull-up counter and a second predriver adapted to receive a data signal and coupled to the pull-down counter as set forth in claim 12, the specifics of the method comprising presetting the drive strength count to a value programmed by a programmable fuse code as set forth in claim 34, adjusting the drive strength count as a function of the drive strength adjustment word comprises incrementing or decrementing an initial value of the count responsive the drive strength adjustment word as set forth in claim 36, the specifics of a method adjusting the drive strength of the output driver as a function of the stored drive strength adjustment word and the drive mode bits as set forth in claim 38, the specifics of means for generating a drive strength count responsive to the drive strength adjustment word and a fuse code as set forth in claim 42, the specifics of a counter coupled to the predriver circuit where the counter has a programmable default value provided to the predriver circuit as the default strength code as set forth in claim 49, and the specifics of the strength code comprising a pull-up drive strength count and a pull-down drive strength count as set forth in claim 52.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arcoleo et al. (US PAT No. 5,864,506) discloses a memory having selectable output strength.

Bridgewater, Jr. (US PAT No. 6,222,388) discloses a low voltage differential driver with multiple drive strengths.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

June 22, 2005